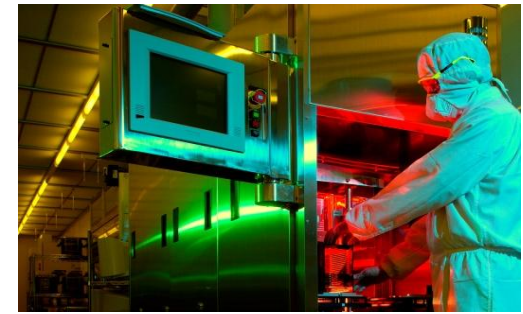
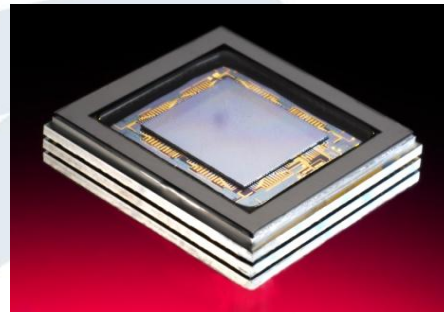
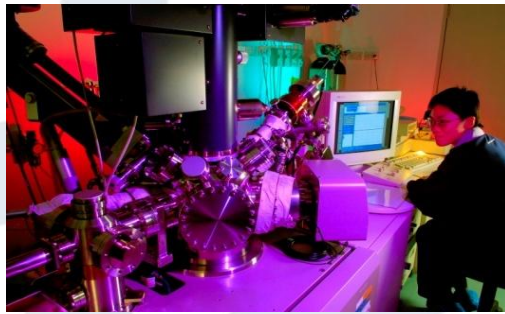




Institute of Microelectronics



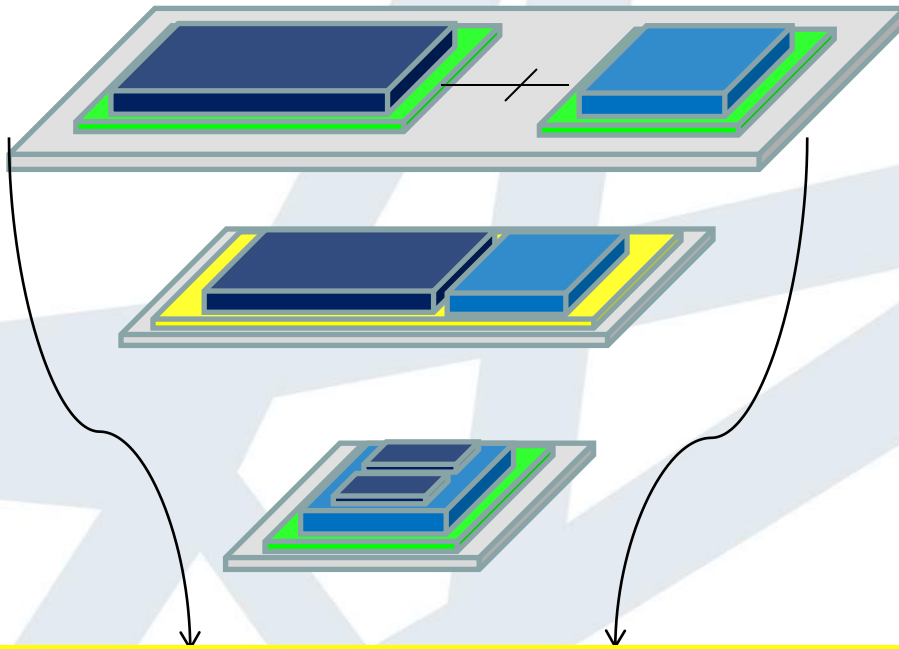
# 3D IC Future in Singapore

Surya Bhattacharya and Dim-Lee Kwong

# OUTLINE

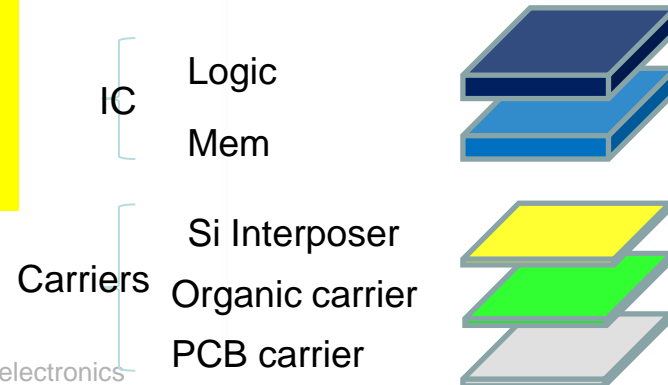
- 2.5D, 3D IC Landscape
- 2.5D, 3D IC Challenges
  - Technology, Manufacturing
  - Design
  - Business Model
- Singapore's 2.5D/3D Ecosystem - IME's value proposition and capabilities to address these challenges.
- Summary

# 2.5D & 3D IC Driving Factors



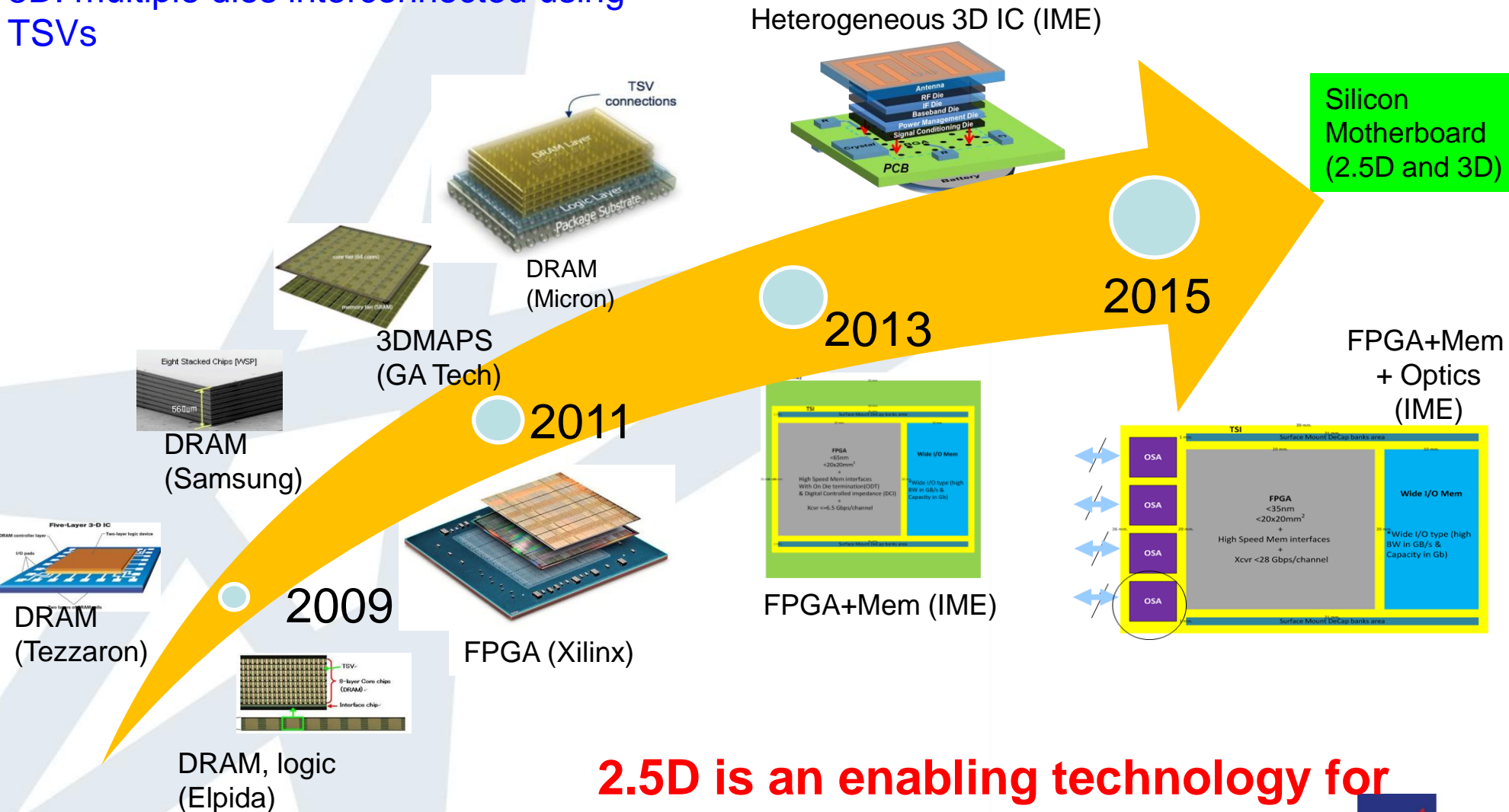
Topology	Form factor	Throughput (#channel* speed)	Power
2D	+	+	+
2.5D	++	++	++
3D	+++	+++	+++

Need for Lower Power, Smaller Form Factor, Higher Performance Drive ICs to 2.5D and 3D.

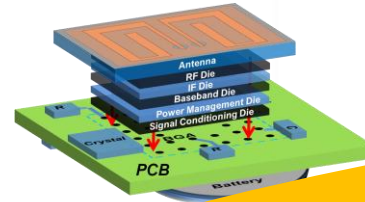


# 2.5D vs. 3D IC Landscape

3D: multiple dies interconnected using TSVs



Heterogeneous 3D IC (IME)



Silicon Motherboard (2.5D and 3D)

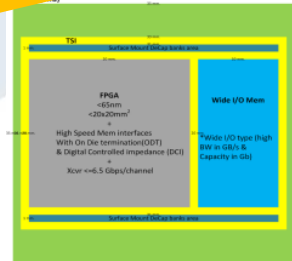
2015

2013

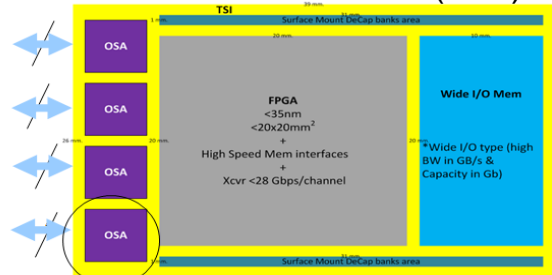
2011

2009

FPGA+Mem + Optics (IME)



FPGA+Mem (IME)



2.5D is an enabling technology for 3D....

# OUTLINE

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- IME's 2.5D, 3D IC Capabilities
- Summary

# Manufacturing Challenges for 2.5D-IC

Challenge

Approach

## Wafer level Over-molding: Warpage issue

- Optimized wafer level molding using new materials
- Warpage correction methods

## Cu protrusion (or pumping)

- Optimized thermal/CMP process
- ECP-Cu grain size control
- TSV/M1 contact structure

## Capacitor integration

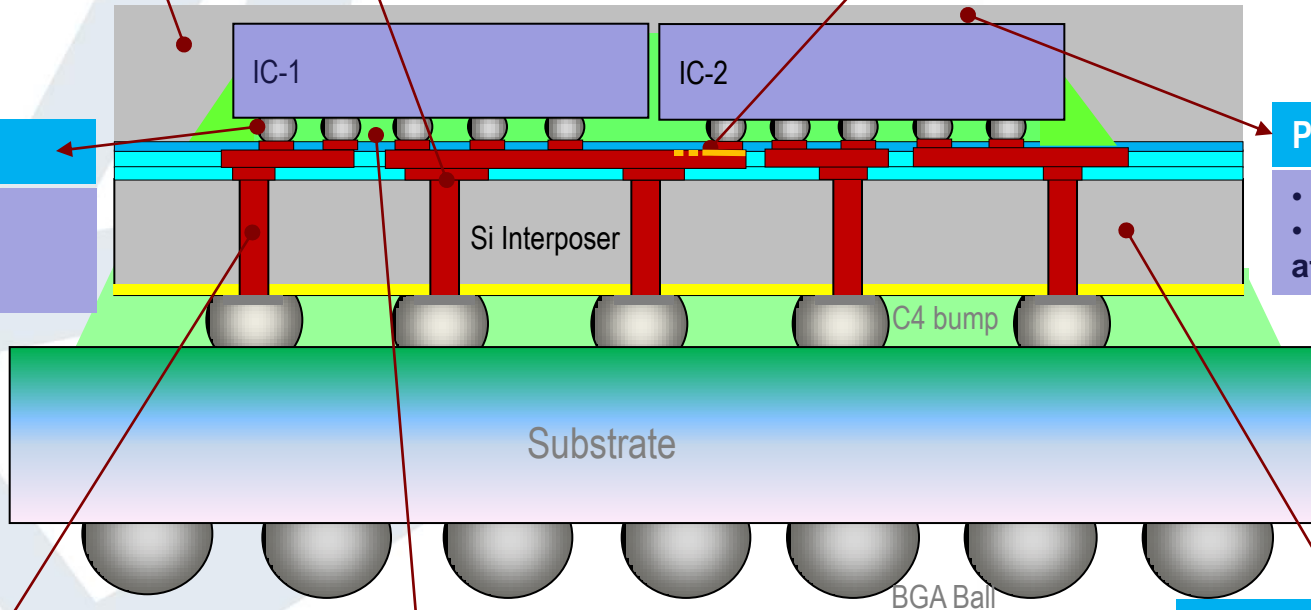
- Thin film process
- BEOL compatible capacitor

## Micro bump joining

- Cu/Solder bump at 30~50um pitch
- C2W bonding

## Poor thermal dissipation

- Molding/Si exposure
- New heat spreader attach



## Stress issue for TSV structure

- Smaller via size
- ECP-Cu grain control
- ILD material for fine RDL

## Underfill for micro bumps

- New capillary UF
- Wafer level UF

## Thin wafer handling

- Carrier with temporary adhesive bonding
- Low cure temperature ILD

# Manufacturing Challenges for 3D-IC

## Wafer level over molding: warpage issue

- Optimized wafer level molding using new materials
- Warpage correction methods

## Cu contamination in Via

- Develop hybrid approach of mechanical grinding and bulk Si etching for via revealing without Cu contamination

## Die stacking using micro bump joining

- Cu/Solder bump at 30~50um pitch
- C2W bonding

## Wafer level bumping and singulation

- Solder ball jetting
- Optimized dicing process for over molded Si wafer

## Thin wafer (50um) handling

- Carrier with temporary adhesive bonding
- Low cure temperature ILD

## Poor thermal dissipation

- Molding/Si exposure
- New heat spreader attach

## Challenge

## Approach

## Underfill for micro bumps In stack module

- New capillary UF
- Wafer level UF

## Process/stress issue for HAR(10:1) TSV structure

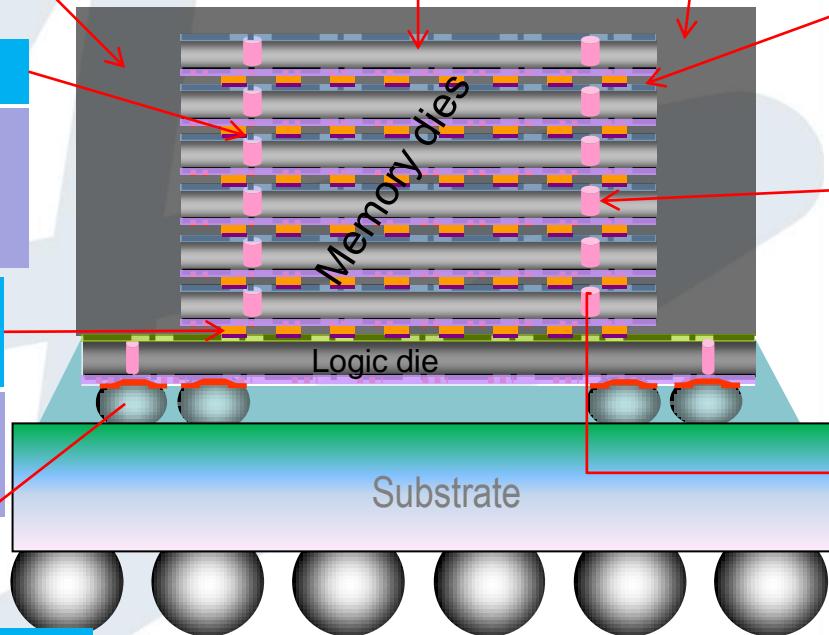
- CuBS process development
- ECP-Cu grain control
- ILD material for fine RDL

## Cu protrusion (or pumping) during BEOL process

- Optimized thermal/CMP process
- ECP-Cu grain size control
- TSV/M1 contact structure

## Testing

- Device performance
- Yield
- Reliability and FA

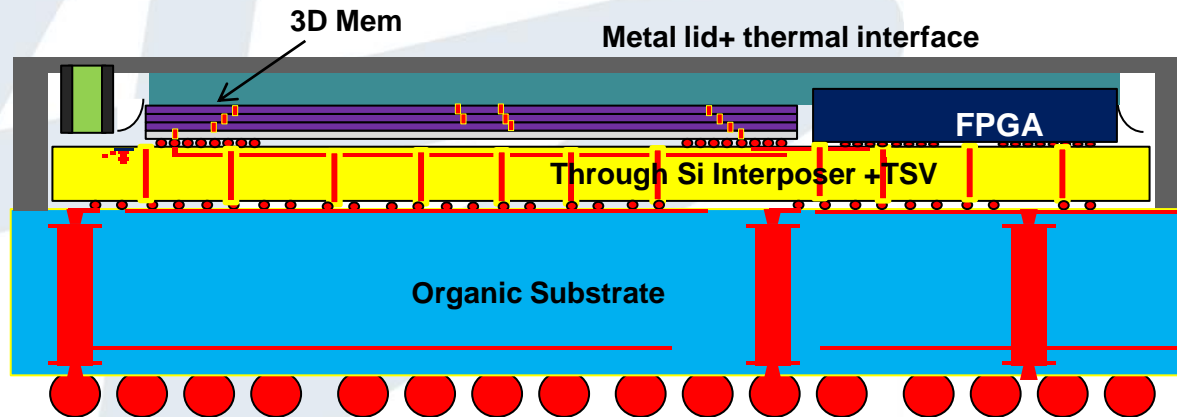


# 2.5D Design Considerations and Challenges

- Power Integrity
  - Decoupling
  - Integrated R,L and C
  - BEOL Wire thickness

## • Architectures

- Applications: High-speed computing, Networking
- Logic Centric vs. Memory Centric
- Cost vs. Performance



- Tools and Standardized Design Flow

- Optimization for low cost applications: Mobile/tablet.

# Challenges for Heterogeneous 3D Integration

## Thermal Management

- Thermal-Vias

## Electromagnetic Interference

- Isolation Techniques

## Signal Distribution

- Serial/Parallel Bus

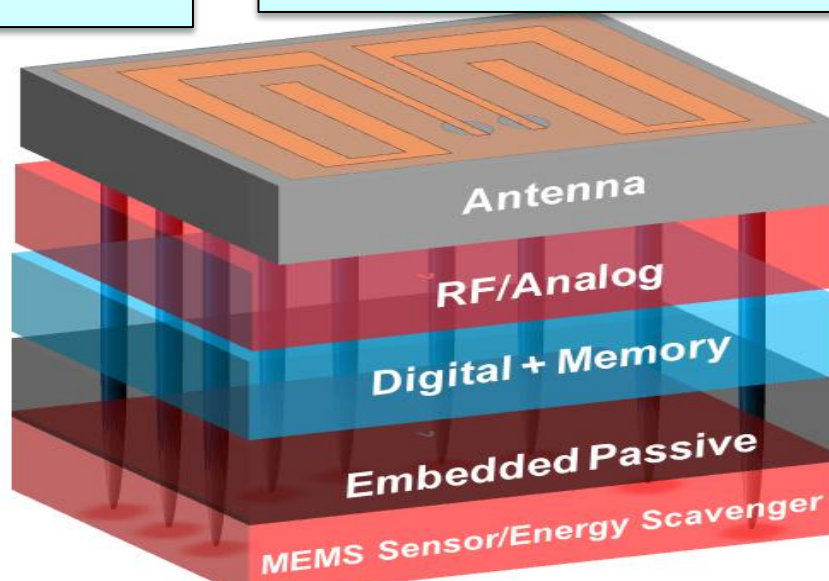
## Design Flow

## Electrical and Mechanical Reliability

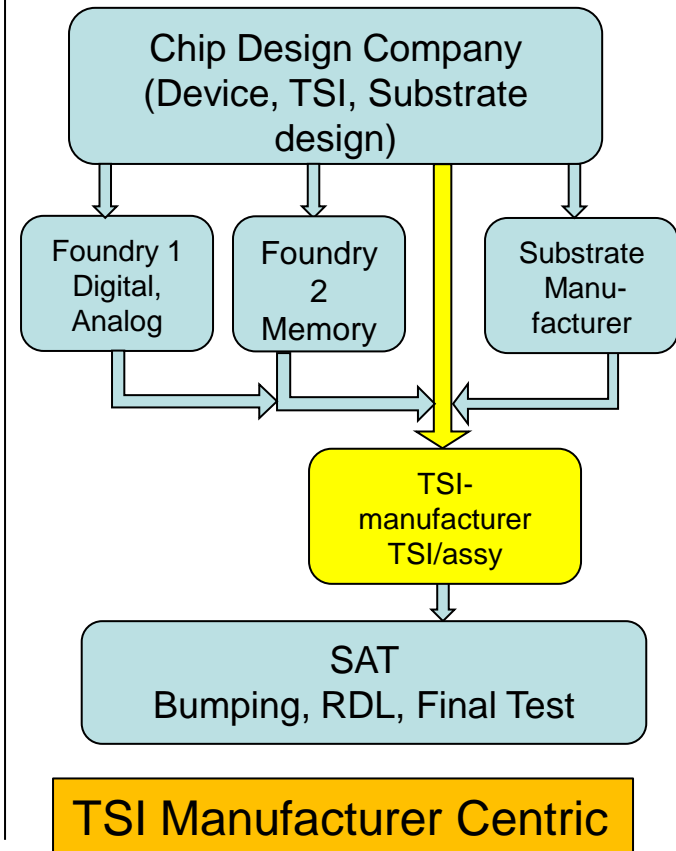
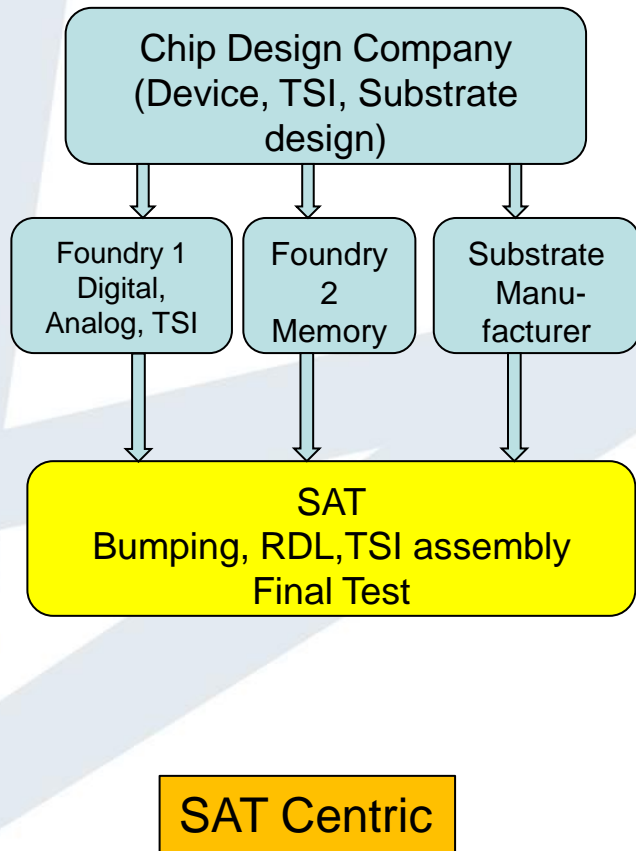
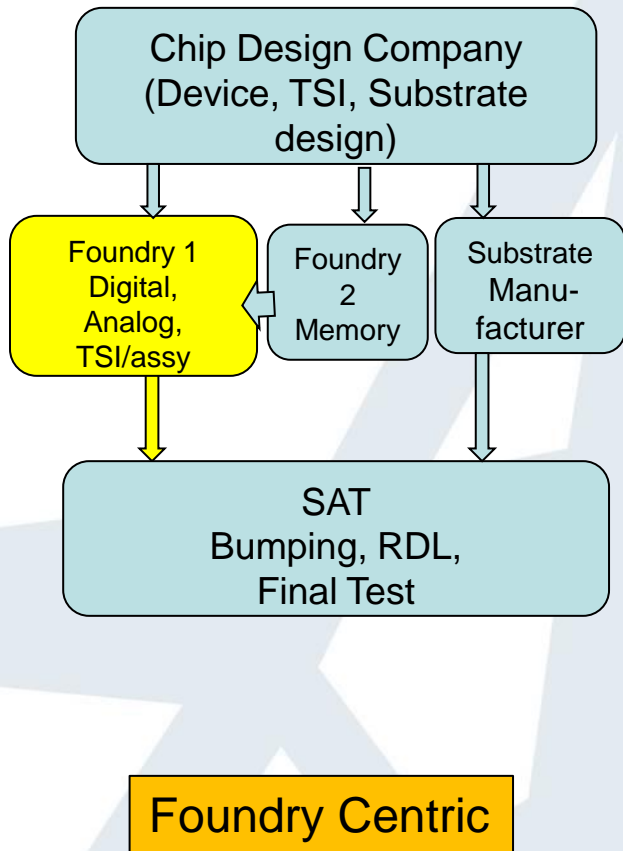
- TSV induced stress effects

## Testing

- Pre/mid/Post-bond



# 2.5D, 3D Business-Model Challenges

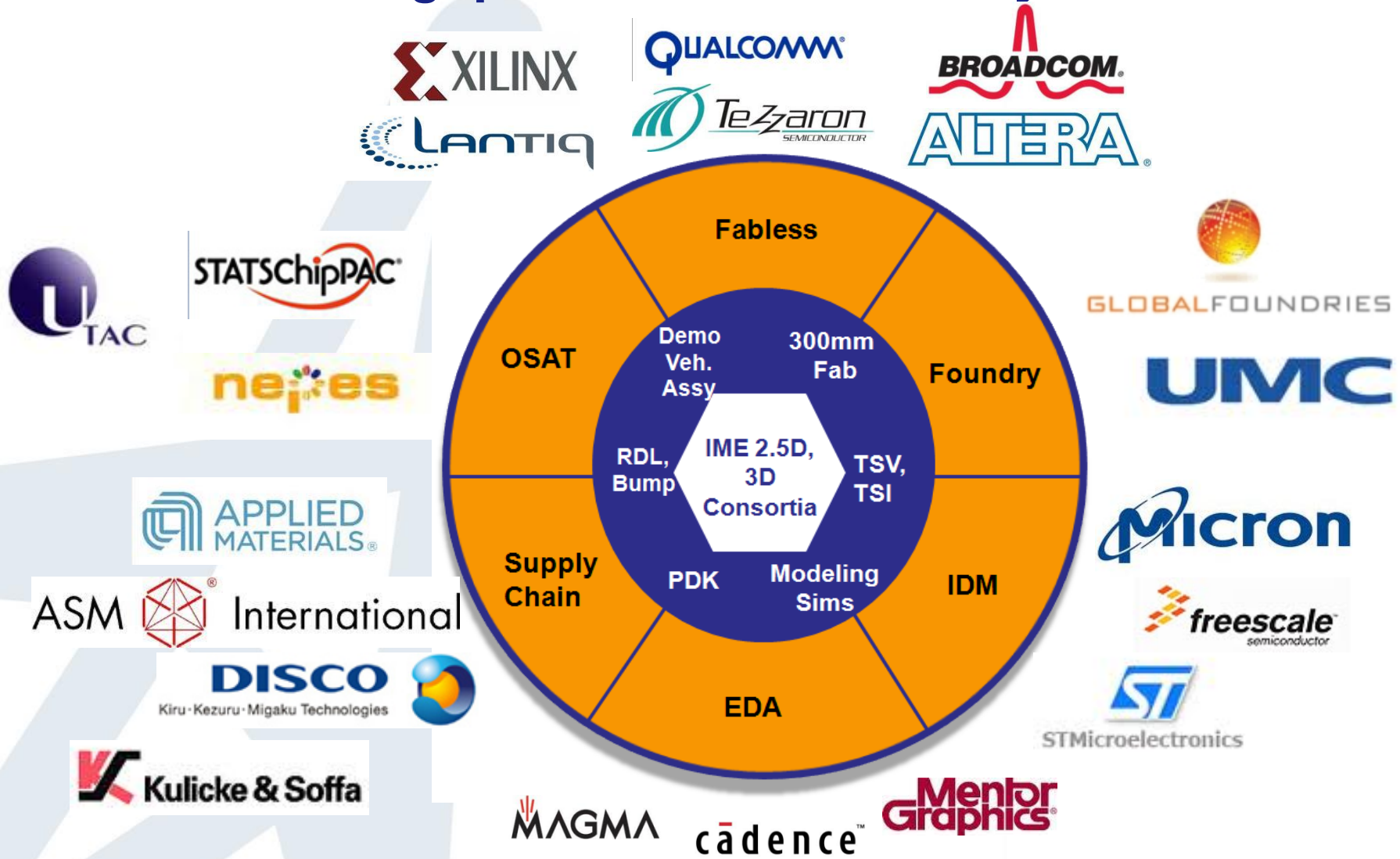


- Industry trying to figure out which model is optimal
- Key business challenge: How to collaborate and co-exist in the 2.5D, 3D ecosystem – and - manage ownership of a “bad 3D/2.5D die” at final test.

# OUTLINE

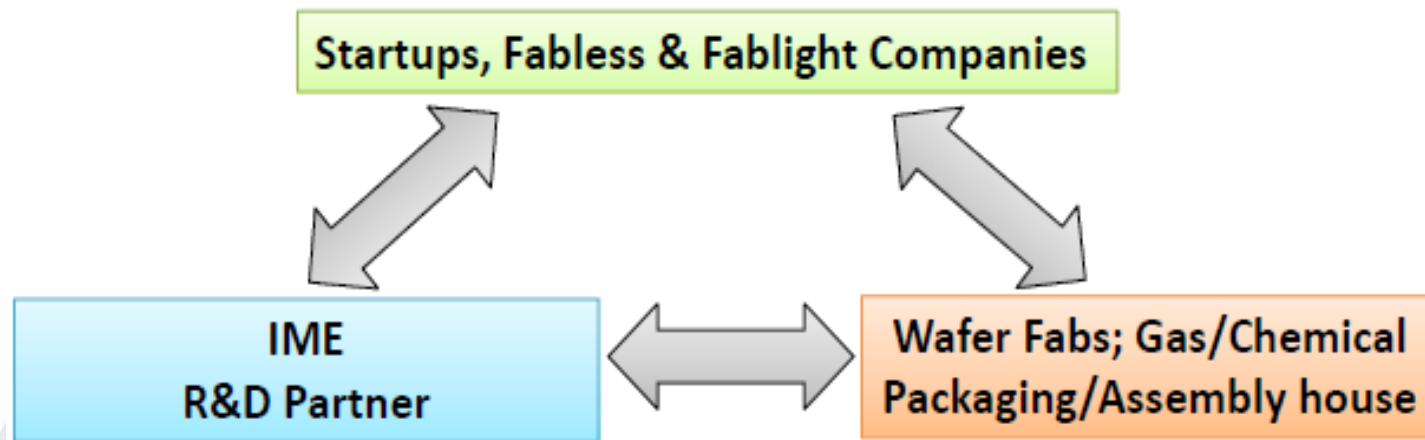
- 2.5D, 3D IC Landscape
- 2.5D, 3D IC Challenges.
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# Singapore's 2.5D, 3D Ecosystem



**IME's role: Provide technology capability and collaborative leadership**

# IME's Value Propositions for 2.5D and 3D Ecosystem



## ■ Multiple-Party Collaborative Business Model

- Bridge gaps between Chip Company, Foundry, Substrate-manufacturer, SAT for 2.5D/3D ICs to allow for seamless manufacturing.
- Address business-model challenges through meaningful partitioning of manufacturing and testing in volume production for 2.5D, 3D ICs.

## ■ Capabilities and Technology Portfolios in “More Than Moore”

- Developing transferable production-worthy **technology platform**
- Demonstrating prototype and its integration into system and products

## ■ Critical Mass for Impactful Cost-effective R&D Partnership

- Small scale pilot runs to enable customers to bring products to markets quickly

# OUTLINE

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# IME 2.5D, 3D IC Platform

200/300 mm fabrication

- TSV formation, (TSV Via size/TSV depth 10um/100um)
  - Si etch
  - TSV liner
  - Barrier/Seed PVD, Cu ECP, CMP.
- BEOL process with Cu Interconnects
- Integrated passives: Resistor, Capacitor, Inductor.

RDL, Bumping, PKG Assembly

- Cu pillar + SnAg Micro-Bump (30um pitch)
- Multi-layer RDL processing
- C2W & C2C bonding
- Wafer thinning (50um), underfilling and Molding
- Thin wafer handling for 12" TSV wafer (50um)

Modeling, Simulation

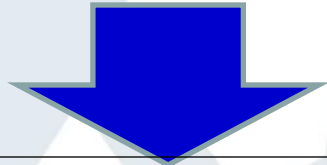
- Mechanical
  - Stress & warpage analysis
  - Solder joint rel. & life prediction
- Thermal
  - Cooling solutions to extract heat from the 3D – IC module
  - Passive cooling design for power density < 10W/cm<sup>2</sup>
- Electrical
  - Schematic/simulation with 3D Full wave solver
  - Signal/Pwr Integrity.

Process Design Kit (PDK)

- Design Rules Manual (DRM)
- Cadence design kit
  - Design rule checking
  - LVS in Cadence (inc. spice models)
  - Parasitic extraction
- Standard cells: TSV, BEOL & FS/BS via/wires, Inductors, Metal Resistance, Bonds (uBps, C4 Bps, Solder balls)
- I/O library: To be implemented in Cadence Design kit

Applications, Vehicles

- Low Cost
- Mobile processor + GPU/Wide-bus Memory on TSI
  - Remove Organic substrate to reduce cost.
- High Performance
- FPGA +Memory
  - Ongoing: OEIC.
  - Cu BEOL interconnect Heterogeneous 3D
  - Wireless sensor node



Litho

DRIE

CVD

Temporally Bond/Debond

Backside Via Revealing

Cu + solder Micro-bumping

Wafer level Underfilling

PVD

ECP

CMP

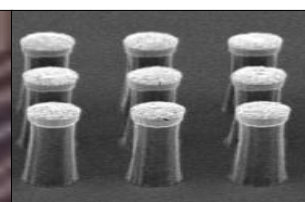
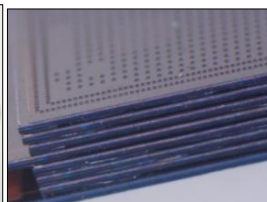
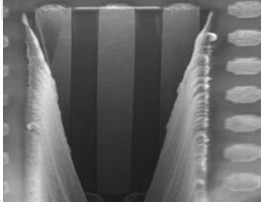
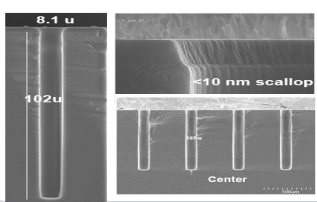
Wafer Thinning

RDL

Wafer molding

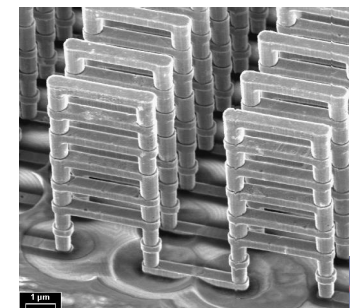
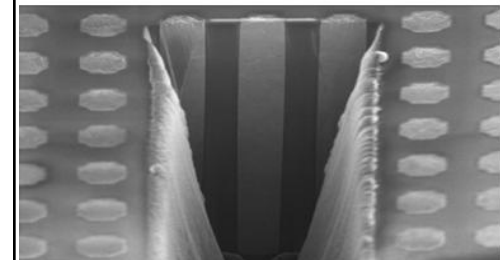
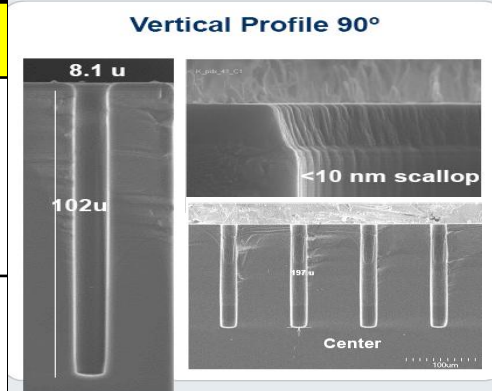
C2W & C2C

Vertical Profile 90°

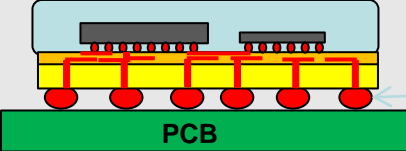
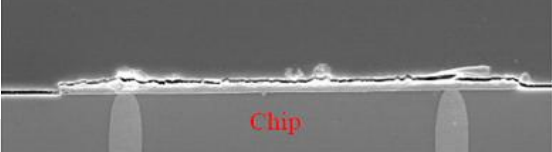
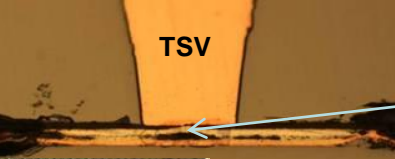
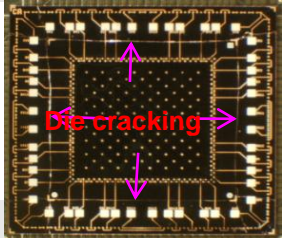

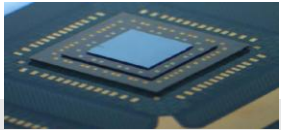
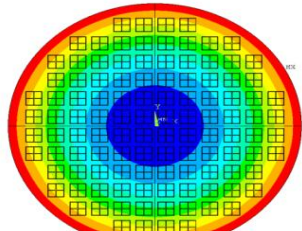
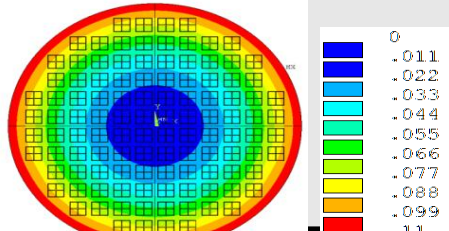


# TSV - Critical Process Modules

Modules	Capabilities	Critical Tools
TSV etch	<ul style="list-style-type: none"> <li>• High aspect ratio ~ 12:1</li> <li>• Vertical Profile ~ 90°</li> <li>• Scallop &lt;10 nm</li> <li>• Etch depth → 100um for 10um Via</li> </ul>	<ul style="list-style-type: none"> <li>• Dielectric/Si/Metal Etcher</li> </ul>
TSV isolation layer process	<ul style="list-style-type: none"> <li>• 180°C PECVD for via-last in 5:1 via</li> <li>• Dielectric performance meets the via middle/via first requirements</li> </ul>	<ul style="list-style-type: none"> <li>• DCVD-Producer GT (Mainframe + chamber A/B)</li> </ul>
TSV via Cu fill, Cu CMP	<ul style="list-style-type: none"> <li>• PVD Seed layer deposition</li> <li>• ECP process; No voids, ~2.5um over-burden with 5um via, ~4um over-burden with 20um via</li> <li>• CMP module; Remove Cu and Ti barrier with &lt;1000A oxide loss; &lt;150A Cu protrusion after CMP</li> </ul>	<ul style="list-style-type: none"> <li>• PVD - Endura</li> <li>• ECP-2 for TSV Plating</li> <li>• CMP -Reflexion LK</li> </ul>
BEOL process	<ul style="list-style-type: none"> <li>• Cu/USG BEOL up to 8 metal layers capability</li> <li>• 0.13um and 0.18 um Single and Dual damascene technology</li> <li>• Cu layer thickness can be up to 3 um.</li> </ul>	<ul style="list-style-type: none"> <li>• DCVD -Producer GT</li> <li>• Dielectric/Si/Metal Etcher</li> <li>• PVD - Endura</li> <li>• ECP-2 for TSV Plating</li> <li>• CMP -Reflexion LK</li> </ul>

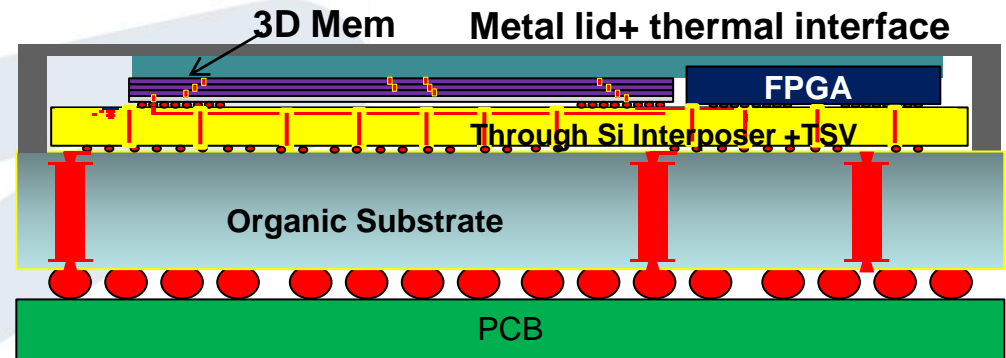


# Modeling Capabilities for Thermo-Mechanical Issues

No.	Issues	IME capabilities	Pictures
1	Board level solder joint reliability	Solder joint reliability analysis and optimization	 <p>Board level solder joints</p>
2	Thin films cracking due to Cu protrusion	Stress analysis (with consideration of the details of metal-1 structure)	 <p>Thin film cracking</p>
3	Solder bump cracking	Novel low stress bond pad design ( i.e., ring pad design)	 <p>Bump cracking</p>
4	TSV die cracking during TSV die stacking	Stress analysis (with different bump layout designs -> to reduce TSV die stress )	 <p>Die cracking</p>  <p>Stress analysis</p>  <p>No cracking in final sample</p>
5	Cracking of TSV wafer	Wafer level stress modeling developed at IME recently	
6	Large warpage of TSV wafer	Wafer level warpage modeling developed at IME recently	

# TSI Demonstration Vehicle (FPGA + Memory)

- Driver: Reduction of transit time between memory and FPGA in high performance networking applications.
- Demo Vehicle
  - Interposer with nominal 4 levels of metal with Cu-BEOL. Size > 25x25 mm<sup>2</sup>,
  - FPGA + 3D memory both in die form mounted on TSI + Organic substrate
  - Thermal solution: air cooled
- Scope:
  - Co-design of TSI and substrate to function with FPGA, memory.
  - TSI fabrication and assembly.
  - Characterization and testing of inter-chip communication performance.



# Photonics IC Building Blocks Proposed on TSI

## ■ Driver:

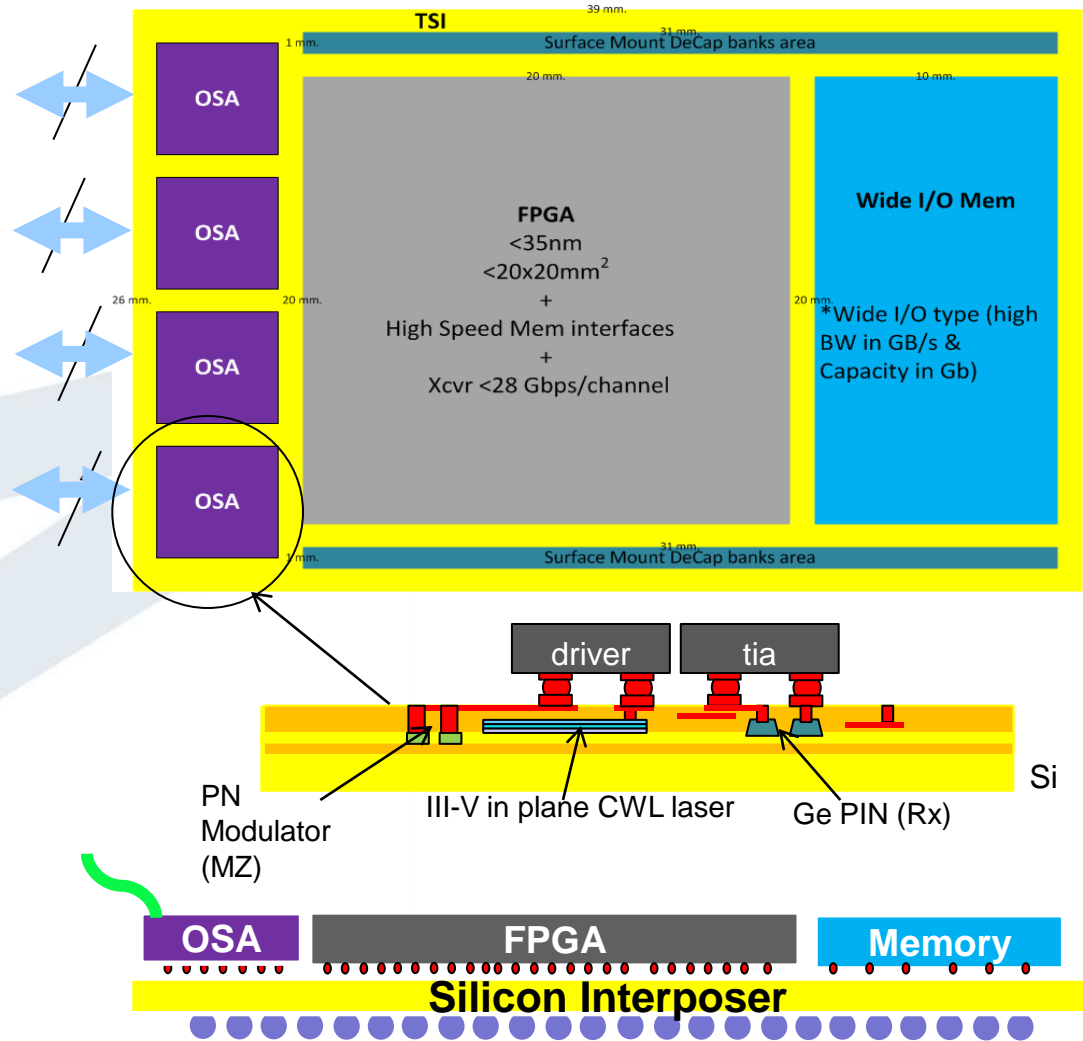
- Reduction of system energy spent on switching in data communication systems.

## ■ Demo vehicle:

- Optical Sub-Assembly (OSA) with integrated hybrid Si laser

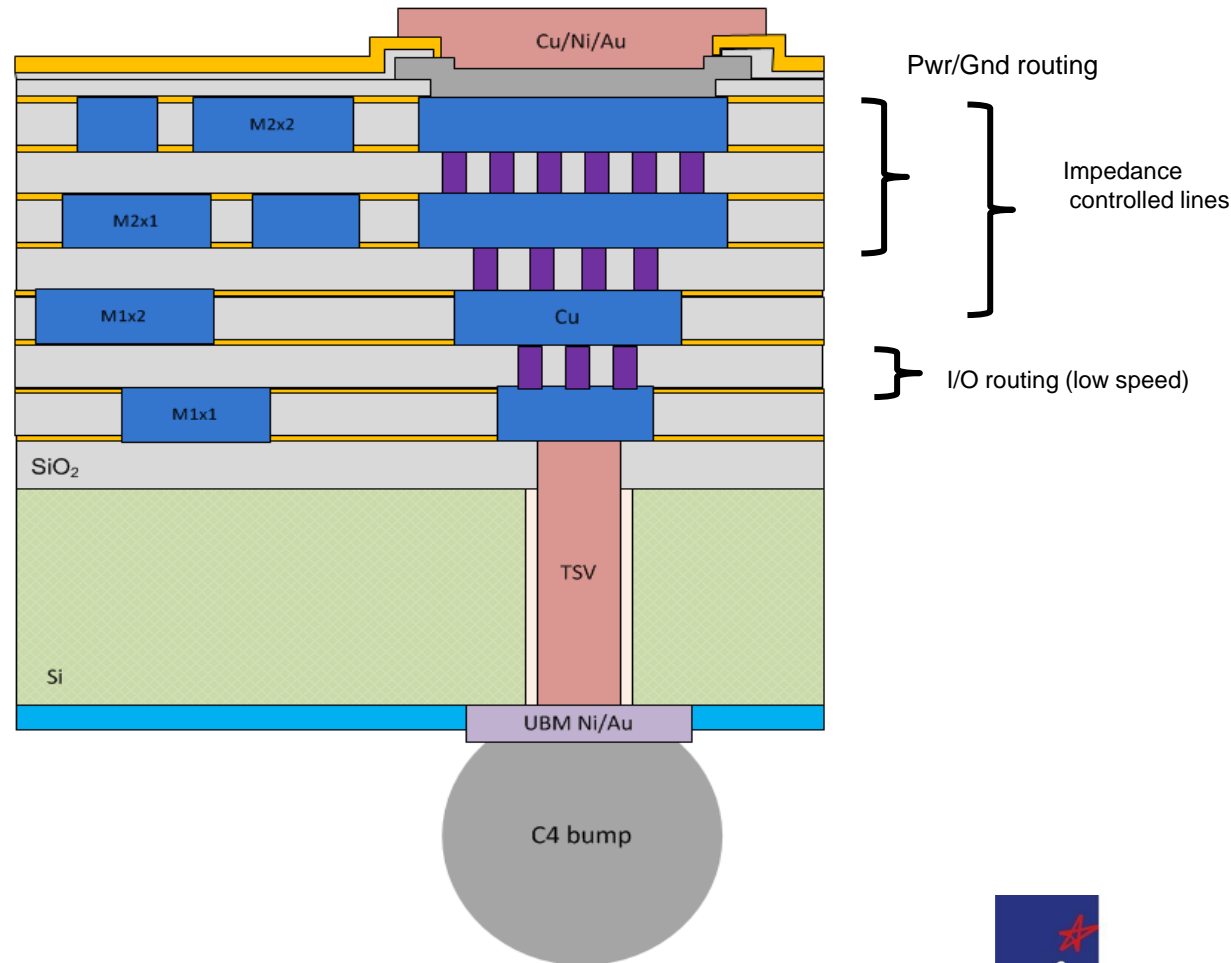
## ■ Approach

- Use IME's extensive experience in CMOS compatible Si Photonics.
- Integration of transmit and receive photonics.
- Develop OSA that matches with the FPGA front-end transceiver.
- Demonstrate readiness to integrate OSA with CMOS-FPGA + memory on TSI.



# Cut-Away of TSI for Demonstration Vehicle

- 4 level of Cu-damascene metal wiring.
- Top 2 layer for power/ground routing
- Top 3 layers for impedance controlled lines
- 2 um Oxide thickness for low wire to wire coupling
- 2um Cu thickness for power distribution
- UBM pad with TSV farm for high power distribution



# TSI Demonstration Vehicle for Mobile/Tablet Applications

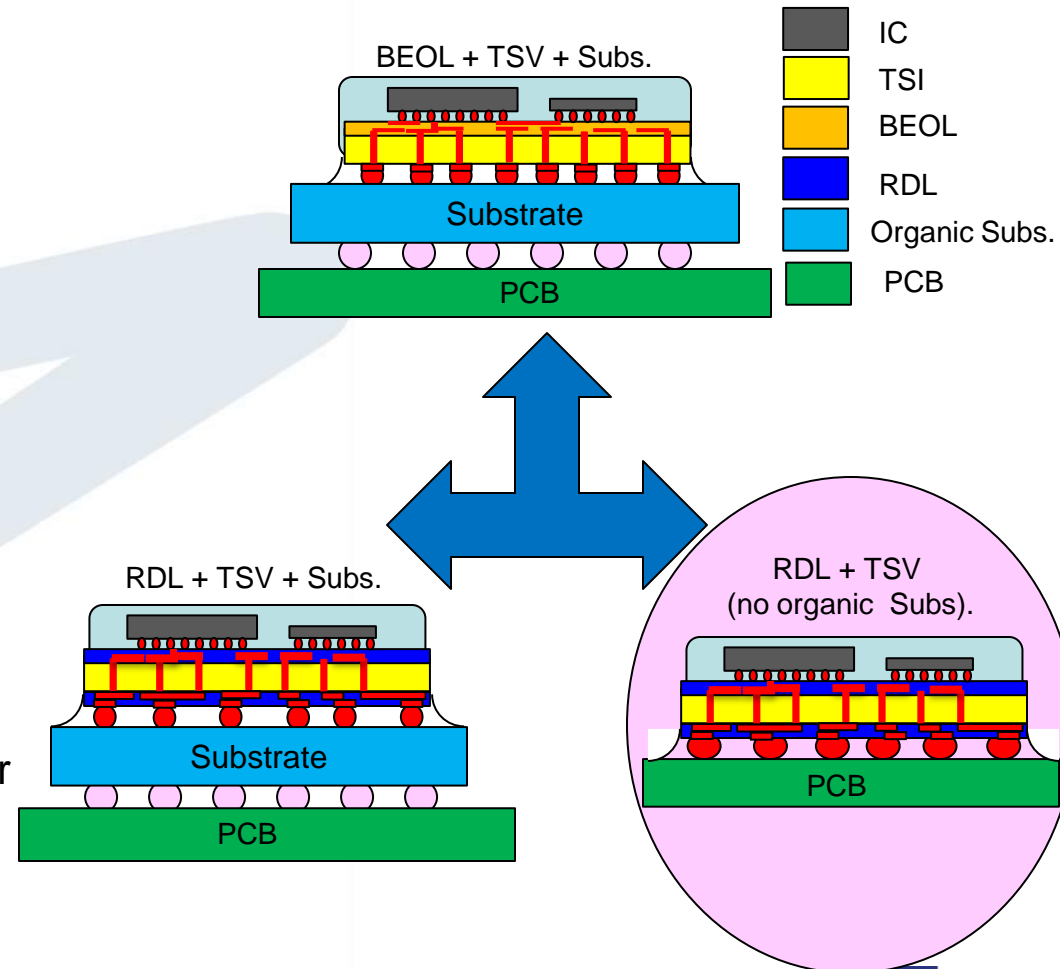
■ Driver: Mobile/tablet TSI applications that are cost-driven.

■ Demo-vehicle:

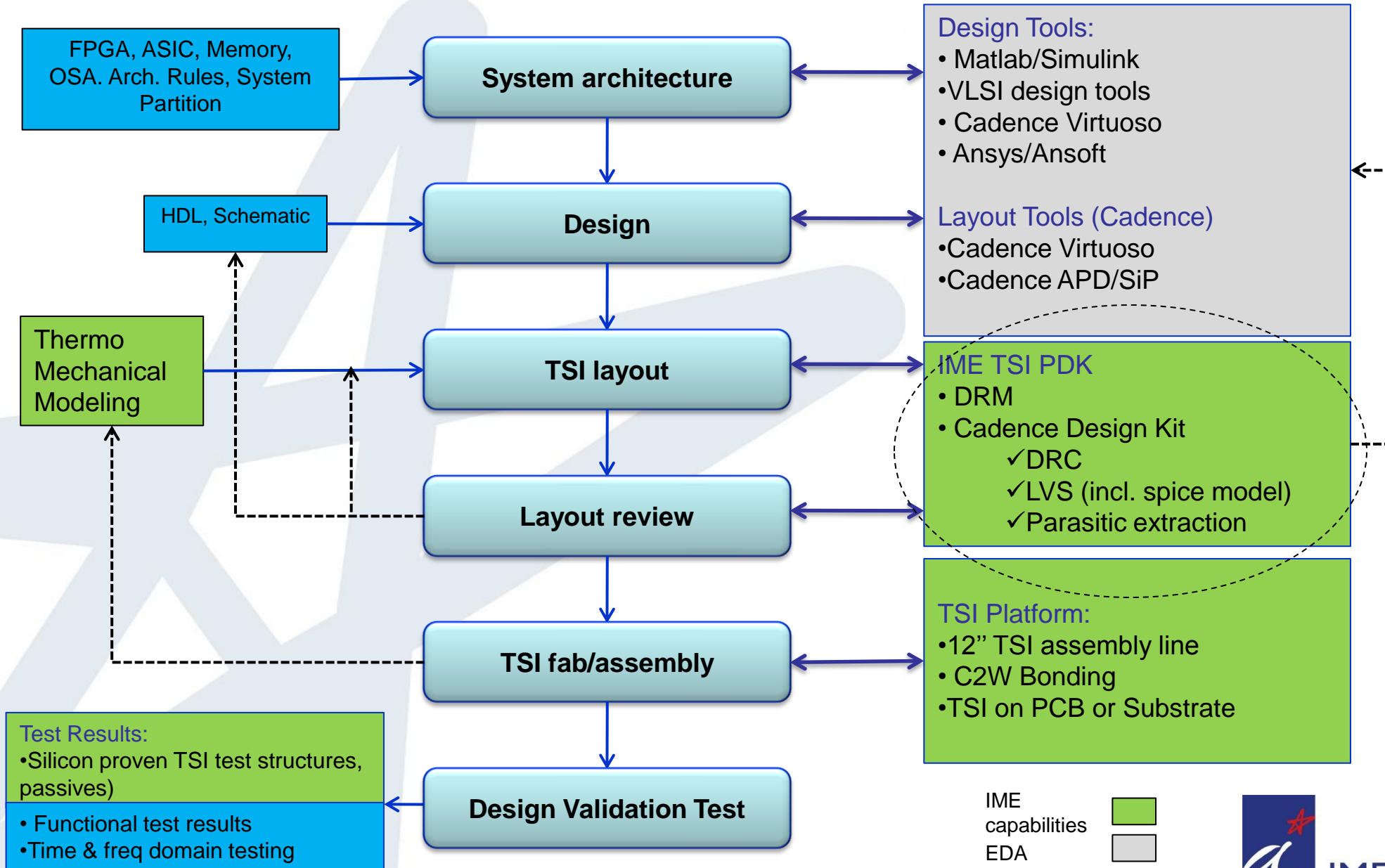
- Interposer with nominal 2 LM on frontside (~ 20x20 mm<sup>2</sup>).
  - CMOS Cu-BEOL vs. RDL on frontside of TSI
  - With vs. without backside RDL
  - With vs. without organic substrate
- Mobile baseband/CPU + GPU OR GPU + memory – integrated on interposer

■ Scope:

- Study feasibility of TSI configurations using electrical/thermo-mechanical simulations for comparison.
- Optimize bonding techniques: chip-to-chip, chip-to-wafer.
- Fabrication, assembly, reliability assessment of low-cost TSI configuration.



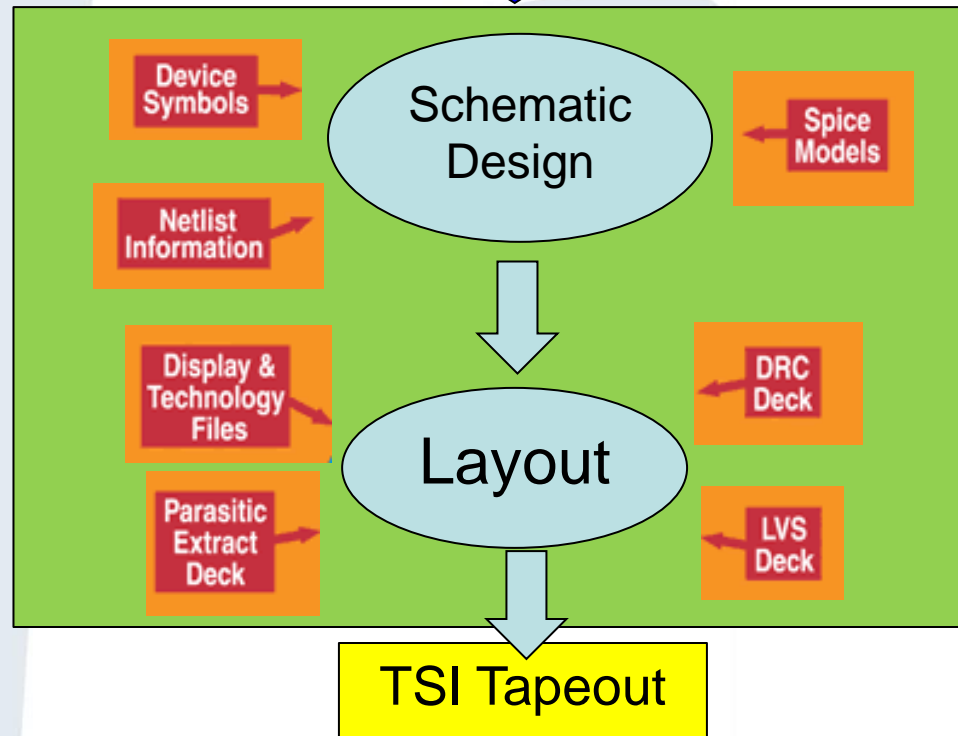
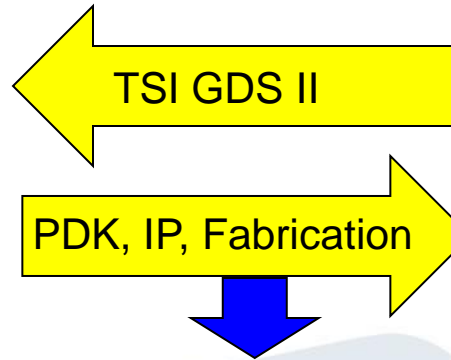
# TSI Design Flow Considerations



# TSI Process Design Kit (PDK) from IME



300 mm Fab



- Process Design Kit (PDK): A key design enabler for 2.5D, 3D ecosystem

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# 3D IC Future in Singapore is Bright

- Singapore's 2.5D, 3D ecosystem has plenty of areas to innovate and excel in design, manufacturing, business-model optimization.
- Collaboration and “More than Moore” technology leadership are critical for 2.5D, 3D IC eco-system. Both are IME's strengths.
- Technology and business-model challenges are viewed by IME as timely opportunities to productively collaborate with industry players for win-win outcome (e.g. IME-AMAT Joint Lab)
- IME will lead and nurture Singapore's ecosystem to ensure Singapore continues as a global technology hub in building 2.5D and 3D ICs.